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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,467	02/26/2004	Kristopher Craig Whitney	ROC920030309US1	7026

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IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,467	WHITNEY, KRISTOPHER CRAIG	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Whitney, for a "Method for achieving higher availability of computer PCI adapters" filed February 26, 2004, has been examined.

Claims 1-17 are presented for examination.

Claims 1-17 are rejected under 35 USC § 102.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Eide et al. (U.S. Patent No. 6,529,978).

As per claim 1, Eide discloses a computer system comprising:

a system processor (Fig. 2, element 12)

an input/output processor (Fig. 2, element 44)

an input/output adaptor (Fig. 2, element 46) connected to the system processor and the input/output processor, and capable of dynamically switching between being controlled by the system processor and being controlled by the input/output processor

(Fig. 12).

As per claim 2, Eide discloses the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2, elements 44, 48).

As per claim 3, Eide discloses the input/output processor is a PCI-compatible processor (Fig. 2, elements 44, 48).

As per claim 4, Eide discloses a method for fault recovery in a computer system having a system processor (Fig. 2, element 12), an input/output processor (Fig. 2, element 44), and an input/output adaptor (Fig. 2, element 46) connected to the system processor and the input/output processor (Fig. 2) that is capable of dynamically switching between being controlled by the system processor and being controlled by the input/output processor(Fig. 12) the method for fault recovery comprising:

detecting a fault in the input/output processor (Fig. 12, element 182)

switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected (Fig. 12, element 184).

As per claim 5, Eide discloses the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2, elements 44, 48).

As per claim 6, Eide discloses the input/output processor is a PCI-compatible processor (Fig. 2, elements 44, 48).

As per claim 7, Eide discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 46) and each of the dynamically switchable input/output adapters being controlled by the input/output processor (Fig. 2, element 44) when the fault is detected is switched to control by the system processor (Fig. 12).

As per claim 8, Eide discloses detecting correction of the fault in the input/output processor (Fig. 12) and (col. 10, lines 38-40)

switching the input/output adapter to control by the input/output processor when the correction of the default is detected, if it was previously switched to control by the system processor as a result of the fault in the input/output processor (col. 10, lines 38-40).

As per claim 9, Eide discloses the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2, elements 44, 48).

As per claim 10, Eide discloses the input/output processor is a PCI-compatible processor (Fig. 2, elements 44, 48).

As per claim 11, Eide discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 46) and each of the dynamically switchable input/output adapters being controlled by the system processor (Fig. 2, element 12) when the correction of the fault is detected is switched to control by the input/output processor if it was previously switched to control by the system processor as a result of the fault in the input/output processor (Fig. 12) and (col. 10, lines 38-40).

As per claim 12, Eide discloses a method for optimizing processor utilization in a computer system (col. 11, lines 6-9) having a system processor (Fig. 2, element 12), an input/output processor (Fig. 2, element 44), and an input/output adaptor (Fig. 2, element 46) connected to the system processor and the input/output processor (Fig. 2), which is capable of dynamically switching between being controlled by the system processor and being controlled by the input/output processor (Fig. 12) the method for optimizing utilization comprising:

determining computer system utilization (Fig. 13, element 190) and (col. 11, lines 6-9)

switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second one of the system processor and the input/output processor (Fig. 13, element 196), if it is determined that the first one of the processors is being over utilized (Fig. 13, element 194) and that the second one of the processors has sufficient capacity that switching control of the input/output adapter

will not adversely affect system throughput (Fig. 13, elements 196, 198).

As per claim 13, Eide discloses switching control of the input/output adapter from the first one of the processors to the second one of the processors is further based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time (Fig. 13) and (col. 11, lines 9-15).

As per claim 14, Eide discloses the steps of determining computer system utilization (Fig. 13, element 190) and (col. 11, lines 6-9)

switching control of the input/output adapter based on such determination are repeated at intervals substantially equal to the specified period of time (col. 11, lines 9-17).

As per claim 15, Eide discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 46), and the steps of determining computer system utilization (Fig. 13, element 190) and (col. 11, lines 6-9)

switching control of the input/output adapter based on such determination are performed for each of the plurality of input/output adapters (Fig. 13).

As per claim 16, Eide discloses the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2, elements 44, 48).

As per claim 17, Eide discloses the input/output processor is a PCI-compatible processor (Fig. 2, elements 44, 48).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Lambeth et al. (U.S. Patent No. 6,023,736), "System for dynamically configuring I/O device adapters where a function configuration register contains ready/not ready flags corresponding to each I/O device adapter".

Wallach et al. (U.S. Patent No. 5,889,965), "Method for the hot swap of a network adapter on a system including a dynamically loaded adapter driver".

Jewett et al. (U.S. Patent No. 6,263,452), "Fault-tolerant computer system with online recovery and reintegration of redundant components".

Garnett et al. (U.S. Patent No. 6,587,961), "Multi-processor system bridge with controlled access".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100